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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,829	09/25/2003	Jun Fan	11439 (NCR.0113US)	7323

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,829	FAN ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *11,12 and 20-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-10 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asahi (US Patent No. 6,975,516) in view of Blakely (US Patent No. 6,618,266).

Regarding claim 1, Asahi, in figure 8, discloses a circuit board comprising: an embedded discrete surface mount first decoupling capacitor (804, the capacitor identified with an arrow) mounted on a surface, an embedded discrete surface mount second decoupling capacitor (804, opposite to the first capacitor) mounted to a surface; wherein the first and second decoupling capacitor are aligned generally along the direction and overlapping one another (see figure) to increase an amount of space in the circuit board through which the vias are extendable. Asahi, though, discloses the first and second capacitor mounted on surfaces of the conductive layer, does not explicitly disclose the first capacitor mounted to a surface of the first reference plane layer and the second capacitor is mounted to surface of a second reference plane layer.

Blakely, in figure 3-6, discloses a circuit board comprising: first (102c) and second reference plane (102d) layers; a first decoupling capacitor (104a) mounted to a

surface of the first reference plane layer (102c); a second decoupling capacitor (104c) mounted to a surface of the second reference plane layer (102d), in order to facilitate higher capacitor density without the inductor problems (column 2, line 24-26). Blakely further recites two such sets of capacitors in figure 6 and a grid of capacitor mounted on the circuit board, in figure 7, to achieve better results.

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to use the structure of Blakely in a printed circuit board to increase the capacitor density and to avoid the inductor problem associated with the capacitors.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Asahi with the first and second capacitors mounted to a surface of the first reference plane layer and second reference plane layer respectively, as taught by Blakely, in order to increase the capacitor density and to avoid the inductor problem associated with the capacitors.

Regarding claim 2, the modified assembly of Asahi further discloses the vias comprise through-hole vias that extend from one side of the circuit to another side of the circuit board, (one shown on right side of partial figure 8).

Regarding claim 3, the modified assembly of Asahi further discloses additional first decoupling capacitors mounted to the surface of the first reference plane layer, and additional second decoupling capacitors mounted to the surface of the second reference plane layer, wherein each pair of first and second decoupling capacitors are

aligned generally along the direction such that multiple spaced-apart lines of decoupling capacitors are provided, each line of decoupling capacitors including a respective pair of first and second decoupling capacitors (see Blakely figure 6 and 7, Asahi figure 8).

Regarding claim 4, the modified assembly of Asahi further discloses the vias extend through the circuit board in regions devoid of decoupling capacitors, (see figure 8)

Regarding claim 5, the modified assembly of Asahi further discloses a dielectric layer (dielectric layer between layer 102c and 102d, Blakely et al., figure 6) between the first and second reference plane layers, wherein the first and second decoupling capacitors are separated by at least the first and second reference plane layers and the dielectric layer, and the vias extend through the first and second reference plane layers and the dielectric layer.

Regarding claim 6, the modified assembly of Asahi further discloses each of the first decoupling capacitors includes a first electrode (107a, Blakely) and a second electrode (106a, Blakely), the circuit board further comprising a first buried via (110d, Blakely) electrically contacted to the first electrode (107a, Blakely) of one of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer (see Blakely et al., figure 3-5, column 3, line 61 to column 4, line 10).

Regarding claim 7, the modified assembly of Asahi further discloses each of the second decoupling capacitors (104c, Blakely) includes first (106c, Blakely) and second (107c) electrodes, the circuit board further comprising a second buried via (110c, Blakely) electrically contacted to the first electrode (106c, Blakely) of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer (see Blakely et al., figure 3-5, column 3, line 61 to column 4, line 10).

Regarding claim 8, the modified assembly of Asahi further discloses layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors (figure 8, Asahi).

Regarding claim 9, the modified assembly of Asahi further discloses the first decoupling capacitors are spaced apart with respect to each other across the surface of the first reference plane layer, and the second decoupling capacitors are spaced apart with respect to each other across a surface of the second reference plane layer (Blakely et al., figure 3, Asahi figure 8).

Regarding claim 10, the modified assembly Asahi further discloses

first regions between the spaced apart first decoupling capacitors (region between the capacitors 104a and 104b, Blakely et al., figure 3); and second regions between the spaced apart second decoupling capacitors (region between capacitors 104c and 104 d, Blakely et al., figure 3), the first and second regions being generally aligned along the direction, the vias extending through the circuit board through the first and second regions, (see figure 3 of Blakely and Figure 8 of Asahi).

Regarding claim 13, the modified assembly Asahi discloses all the features of the claimed invention including the first and second reference plane layers; and embedded discrete surface mount first and second decoupling capacitors, as applied to claim 1 above and further recites integrated circuit device (806, 811, figure 8). Regarding the limitation "a power supply", though the modified system of Asahi does not explicitly disclose a power supply, the power supply has to be there for operating the system.

Regarding claim 14, the modified assembly of Asahi further discloses the vias comprise through-hole vias that extend from one side of the circuit board to another side of the circuit board, as applied to claim 2 above.

Regarding claim 15, the modified assembly of Asahi all discloses all the features of the claimed invention as applied to claim 13 above including the through vias as applied to claim 14, above but does not explicitly disclose the vias extending through

the circuit board in regions between spaced apart first and second decoupling capacitors, however, it is considered that there must be vias between spaced apart first and second decoupling capacitor but are not visible as only cross section is shown. Alternately, Asahi discloses the through via as applied to claim 14 above, and would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide as many through via as required, and for that matter even between spaced apart first and second decoupling capacitors, in order to facilitate trace routing and for external connection of the inner layers.

Regarding claim 16, the modified assembly of Asahi discloses all the features of the claimed invention including the circuit board further comprising a dielectric between the first and second reference plane layers, wherein each of the first decoupling capacitors includes a first electrode and a second electrode and wherein the circuit board further comprises a first buried via electrically contacted to the first electrode of one of the decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer as applied to claim 5 and 6 above.

Regarding claim 17, the modified assembly of Asahi further discloses each of the second decoupling capacitors includes first and second electrodes, wherein the circuit board further comprises a second buried via electrically contacted to the first electrode of one of the second decoupling capacitors, the second buried via extending

through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer as applied to claim 7 above.

Regarding claim 18, the modified assembly of Asahi further discloses the circuit board further comprises layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors, as applied to claim 8 above.

Regarding claim 19, the modified assembly of Blakely et al., further discloses first regions between the spaced apart first decoupling capacitors and second regions between the spaced apart second decoupling capacitors, the first and second regions being generally aligned along the direction, the vias extending through the circuit board through the first and second region, as applied to claim 10 above.

Response to Arguments

3. Applicant's arguments with respect to claims 1-10 and 13-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
January 8, 2006